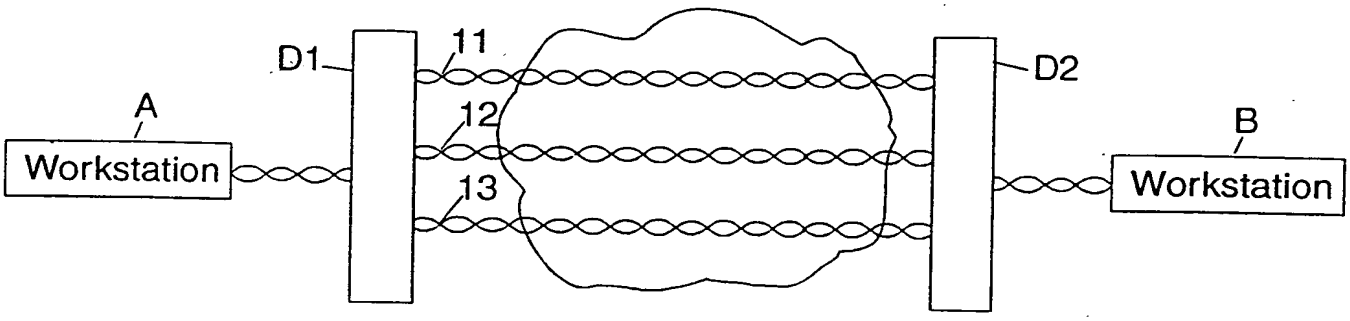
D1
11
D2
A
12
B
Workstation
13
Workstation

FIG. 1

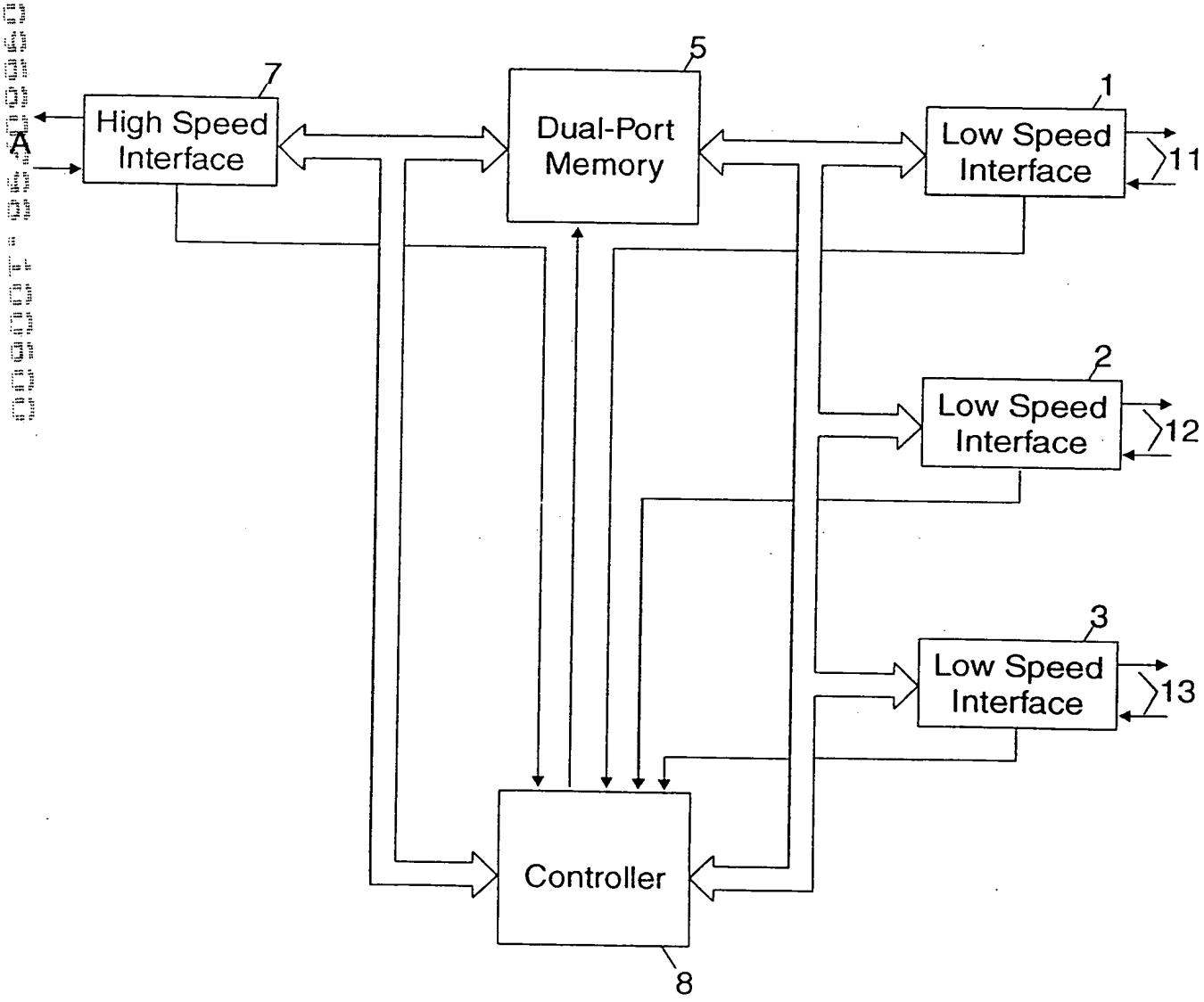
5
7
1
High Speed Interface
Dual-Port Memory
Low Speed Interface
A
11
2
Low Speed Interface
12
3
Low Speed Interface
13
Controller
8

FIG. 2

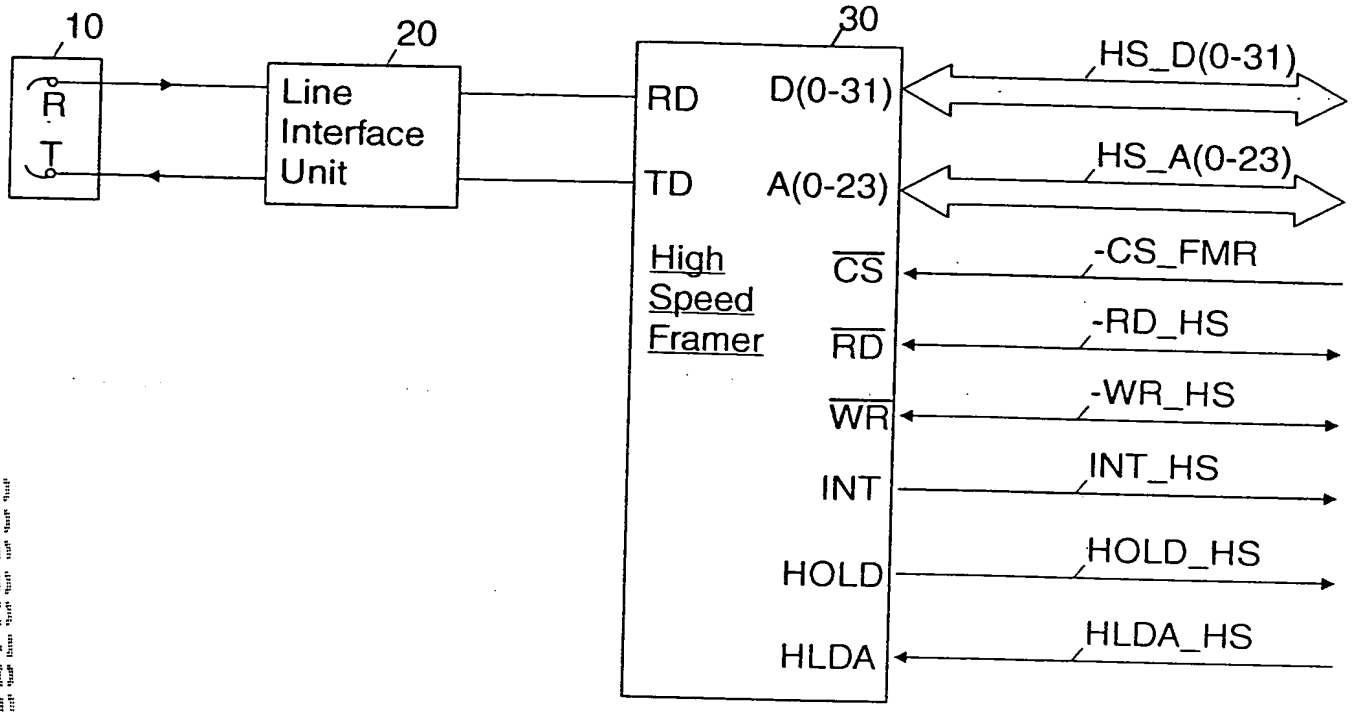
10
R
T
20
Line
Interface
Unit
30
RD
TD
High
Speed
Framer
D(0-31)
A(0-23)
CS
RD
WR
INT
HOLD
HLDA
HS_D(0-31)
HS_A(0-23)
-CS_FMR
-RD_HS
-WR_HS
INT_HS
HOLD_HS
HLDA_HS

FIG. 3

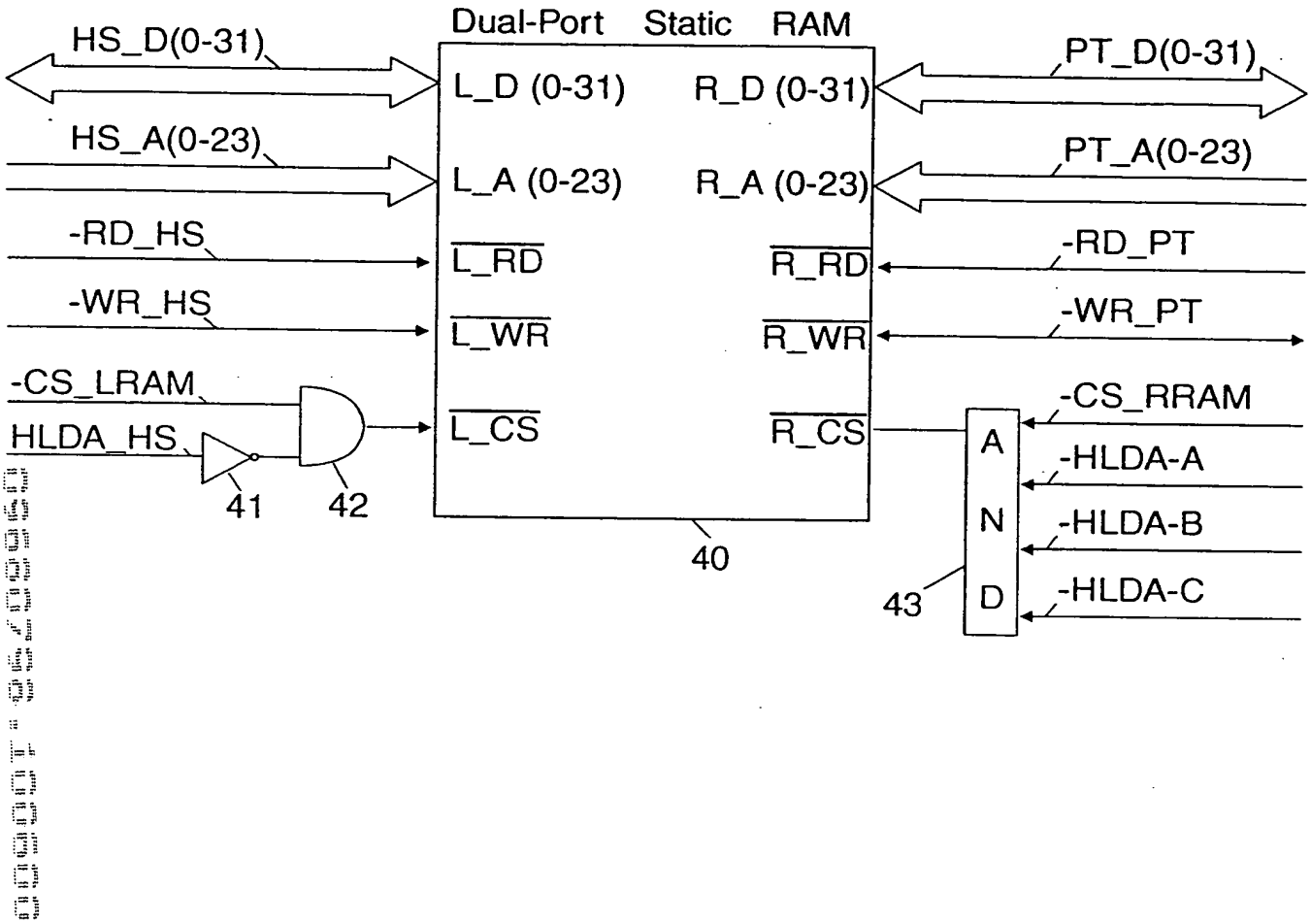
Dual-Port Static RAM
HS_D(0-31)
L_D (0-31)
R_D (0-31)
PT_D(0-31)
HS_A(0-23)
L_A (0-23)
R_A (0-23)
PT_A(0-23)
-RD_HS
L_RD
R_RD
-RD_PT
-WR_HS
L_WR
R_WR
-WR_PT
-CS_LRAM
HLDA_HS
L_CS
R_CS
-CS_RRAM
-HLDA-A
-HLDA-B
-HLDA-C
A
N
D
41
42
40
43

FIG. 4

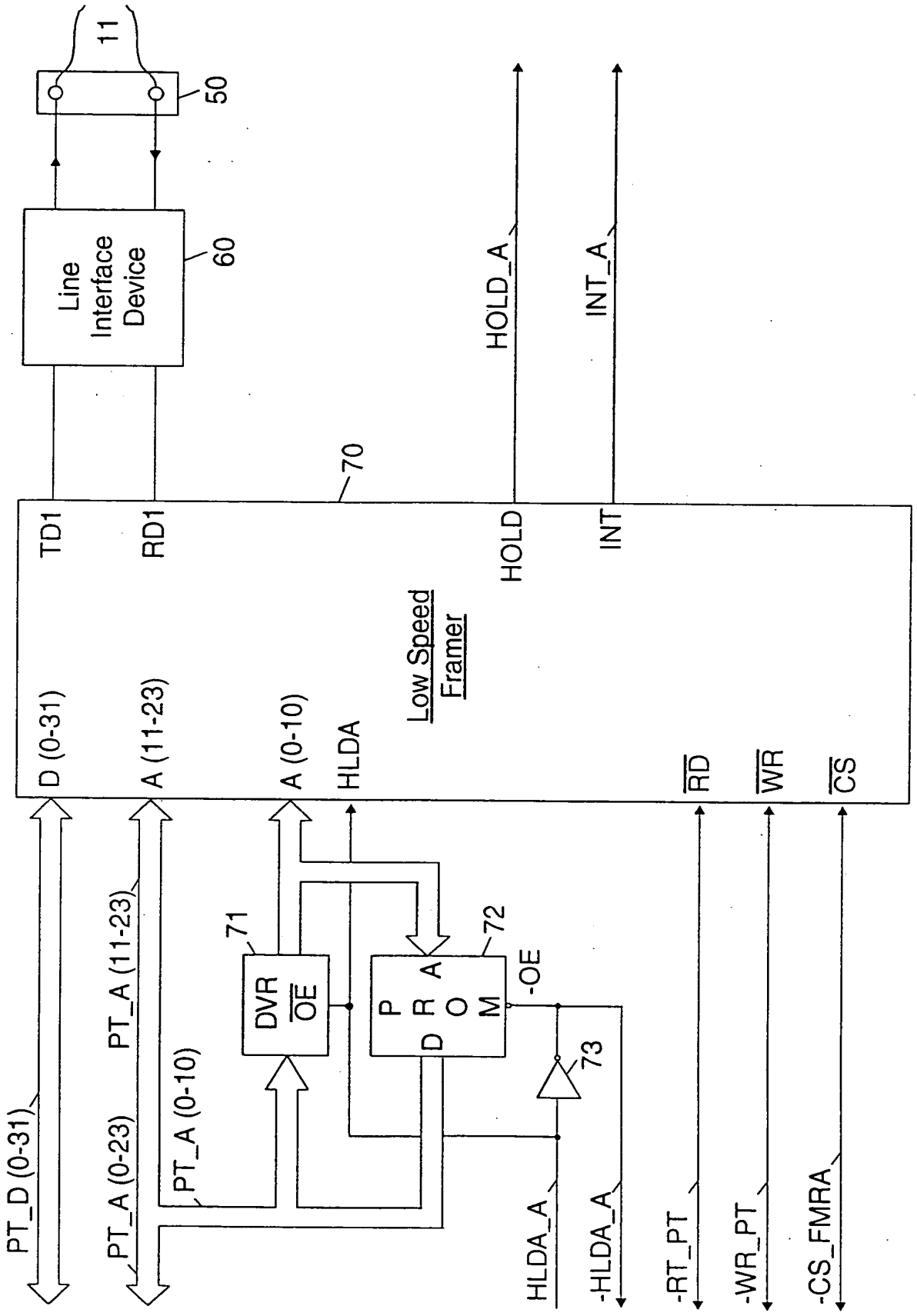
11
50
Line Interface Device
60
HOLD_A
INT_A
70
TD1
RD1
HOLD
INT
Low Speed Framer
D (0-31)
A (11-23)
A (0-10)
HLDA
RD
WR
CS
71
DVR
OE
72
PROM
-OE
73
PT_D (0-31)
PT_A (0-23)
PT_A (11-23)
PT_A (0-10)
HLDA_A
-HLDA_A
-RT_PT
-WR_PT
-CS_FMRA

FIG. 5

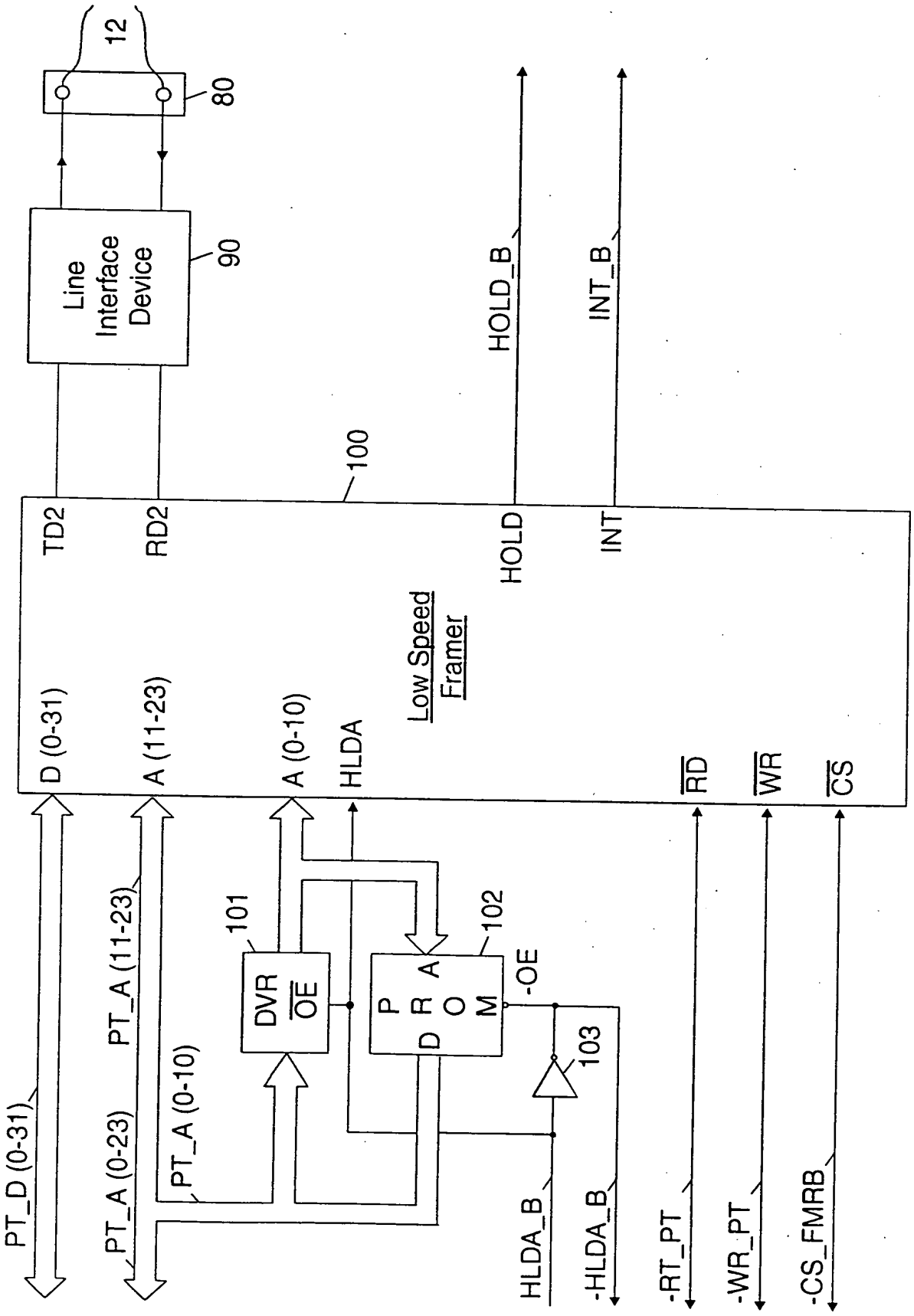
12
80
Line Interface Device
90
HOLD_B
INT_B
100
TD2
RD2
HOLD
INT
Low Speed Framer
D (0-31)
A (11-23)
A (0-10)
HLDA
RD
WR
CS
PT_D (0-31)
PT_A (11-23)
PT_A (0-23)
PT_A (0-10)
101
DVR OE
102
PROM
-OE
103
HLDA_B
-HLDA_B
-RT_PT
-WR_PT
-CS_FMRB

FIG. 6

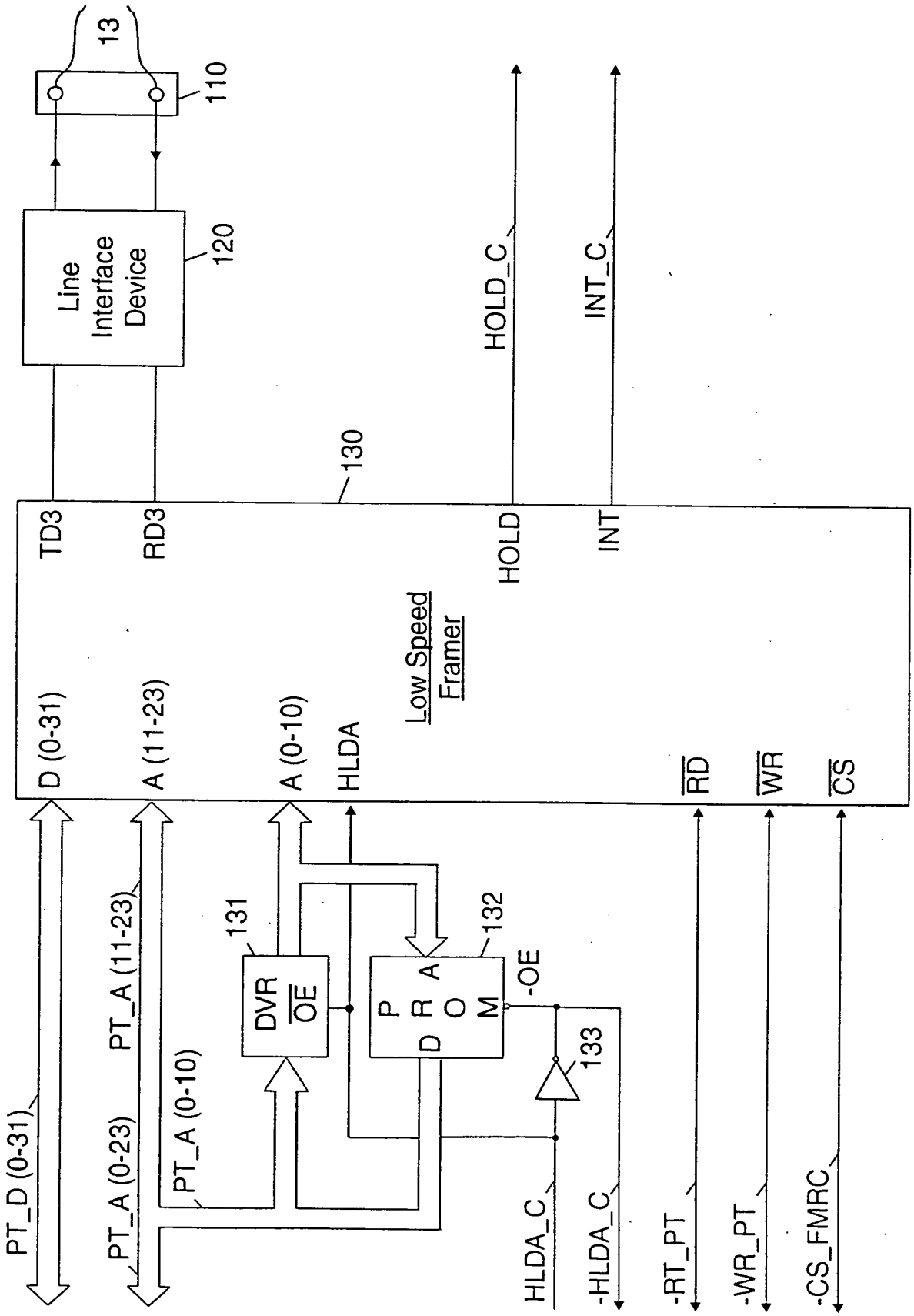
13
110
Line Interface Device
120
HOLD_C
INT_C
130
TD3
RD3
HOLD
INT
Low Speed Framer
D (0-31)
A (11-23)
A (0-10)
HLDA
RD
WR
CS
131
132
DVR
OE
PROM
A
-OE
133
PT_D (0-31)
PT_A (11-23)
PT_A (0-23)
PT_A (0-10)
HLDA_C
-HLDA_C
-RT_PT
-WR_PT
-CS_FMRC

FIG. 7

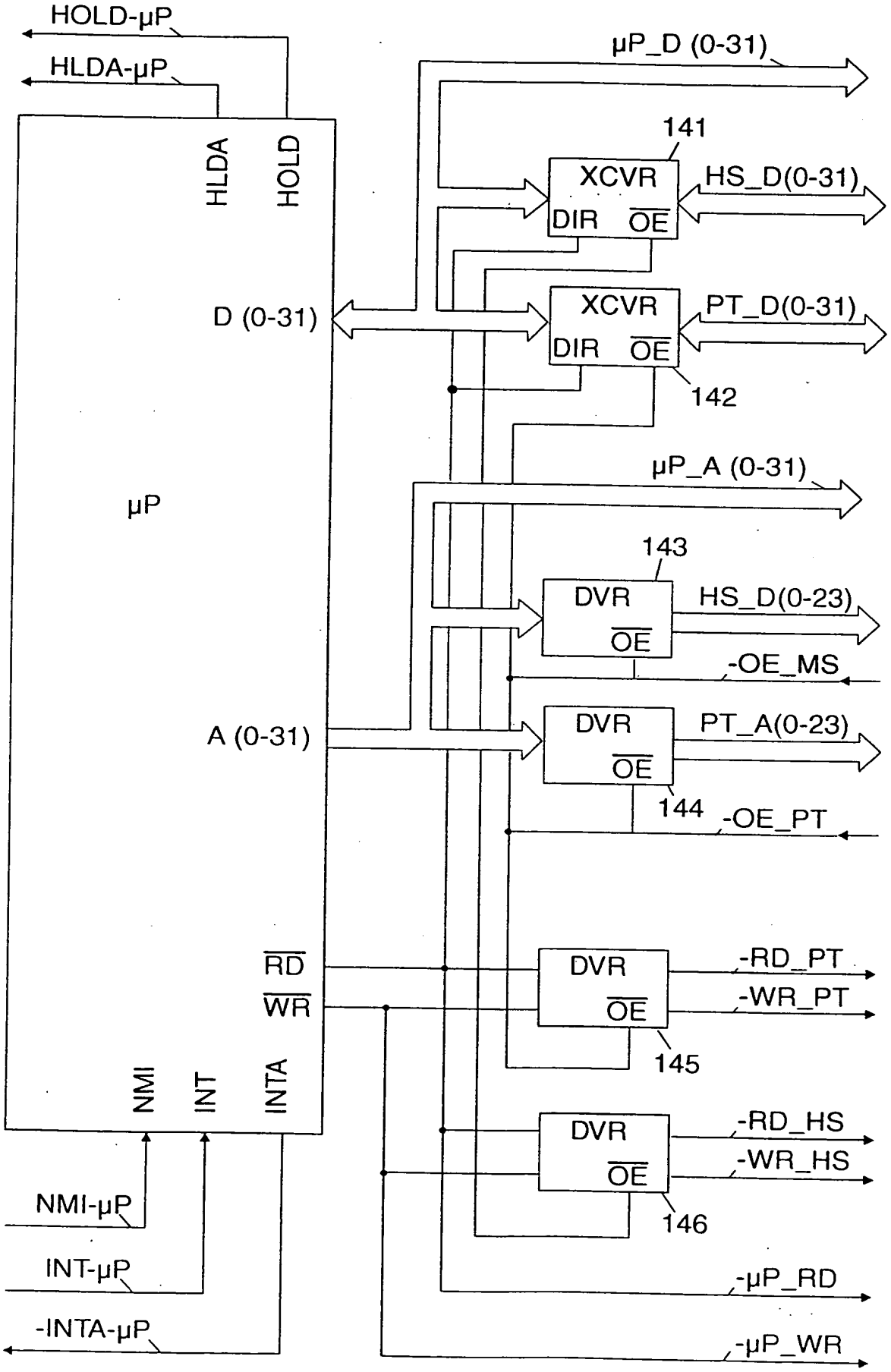
HOLD-µP
HLDA-µP
HLDA
HOLD
µP_D (0-31)
141
XCVR
DIR
OE
HS_D(0-31)
D (0-31)
XCVR
DIR
OE
PT_D(0-31)
142
µP_A (0-31)
µP
143
DVR
OE
HS_D(0-23)
-OE_MS
A (0-31)
DVR
OE
PT_A(0-23)
144
-OE_PT
RD
WR
DVR
OE
-RD_PT
-WR_PT
145
NMI
INT
INTA
DVR
OE
-RD_HS
-WR_HS
146
NMI-µP
INT-µP
-µP_RD
-INTA-µP
-µP_WR

FIG. 8

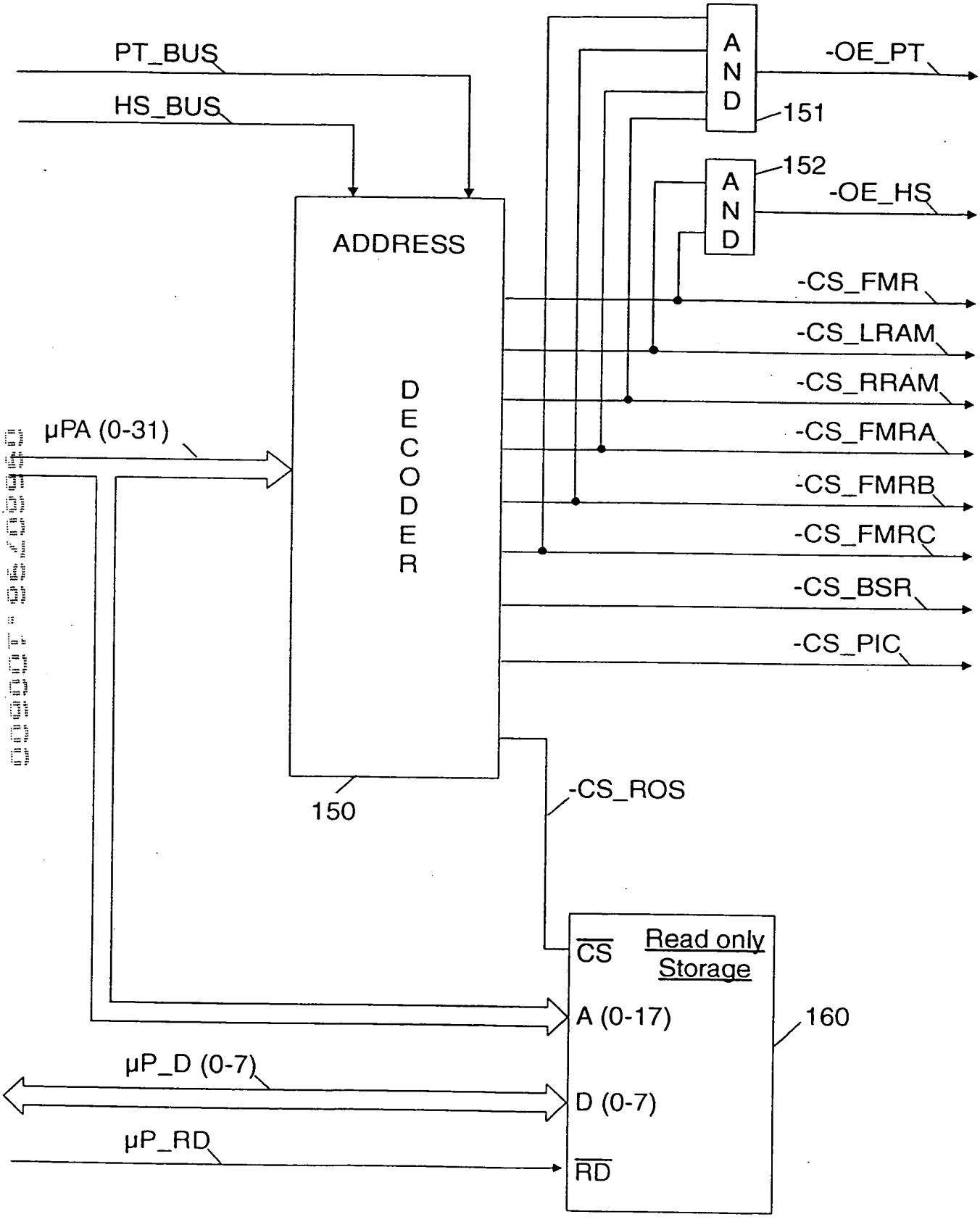
PT_BUS
HS_BUS
ADDRESS
DECODER
150
AND
151
AND
152
-OE_PT
-OE_HS
-CS_FMR
-CS_LRAM
-CS_RRAM
-CS_FMRA
-CS_FMRB
-CS_FMRC
-CS_BSR
-CS_PIC
µPA (0-31)
-CS_ROS
CS
Read only Storage
A (0-17)
160
µP_D (0-7)
D (0-7)
µP_RD
RD

FIG. 9

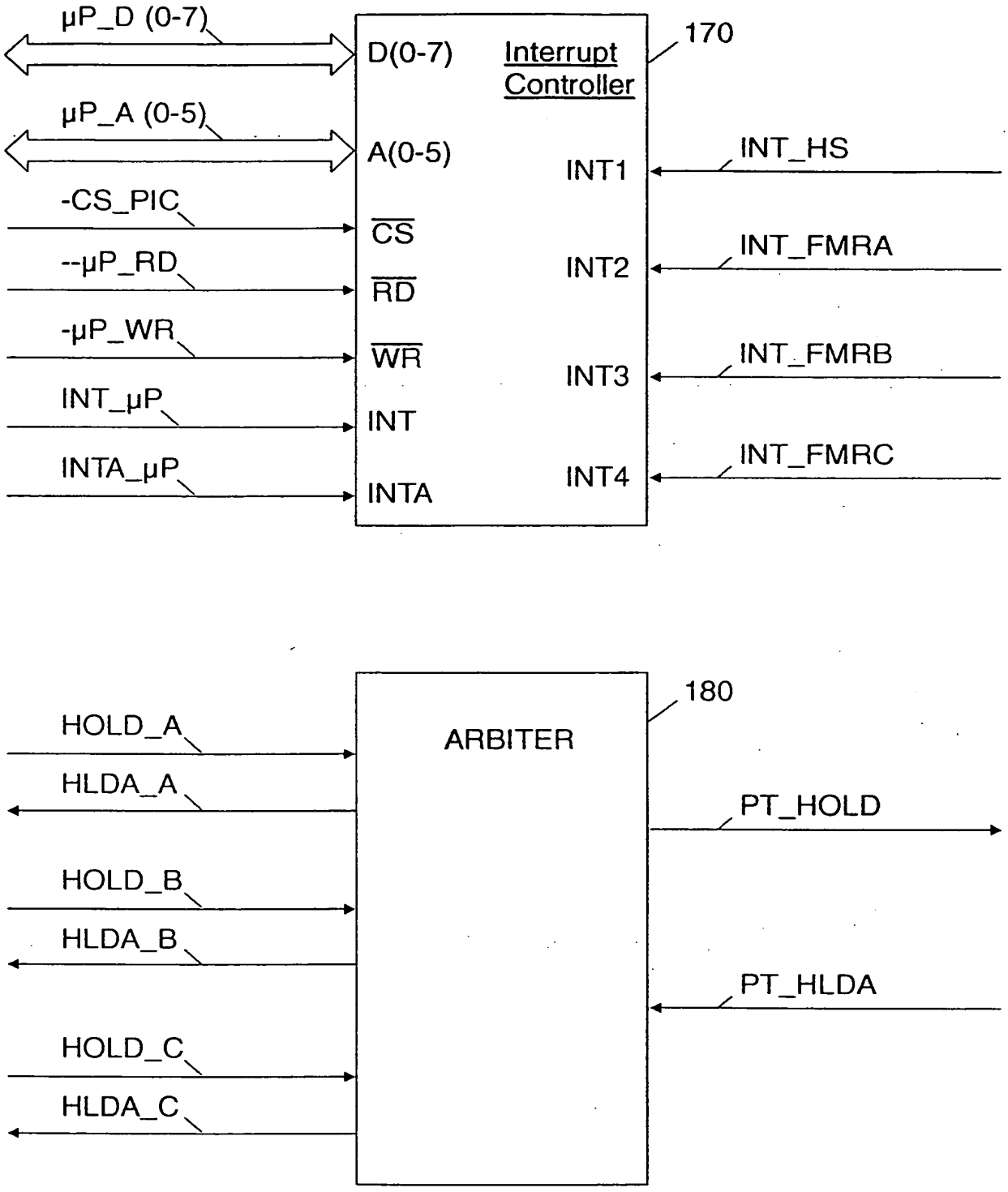
µP_D (0-7)
D(0-7)
Interrupt Controller
170
µP_A (0-5)
A(0-5)
INT_HS
INT1
-CS_PIC
CS
INT_FMRA
--µP_RD
INT2
RD
-µP_WR
WR
INT_FMRB
INT3
INT_µP
INT
INTA_µP
INT_FMRC
INT4
INTA
180
HOLD_A
ARBITER
HLDA_A
PT_HOLD
HOLD_B
HLDA_B
PT_HLDA
HOLD_C
HLDA_C

FIG. 10

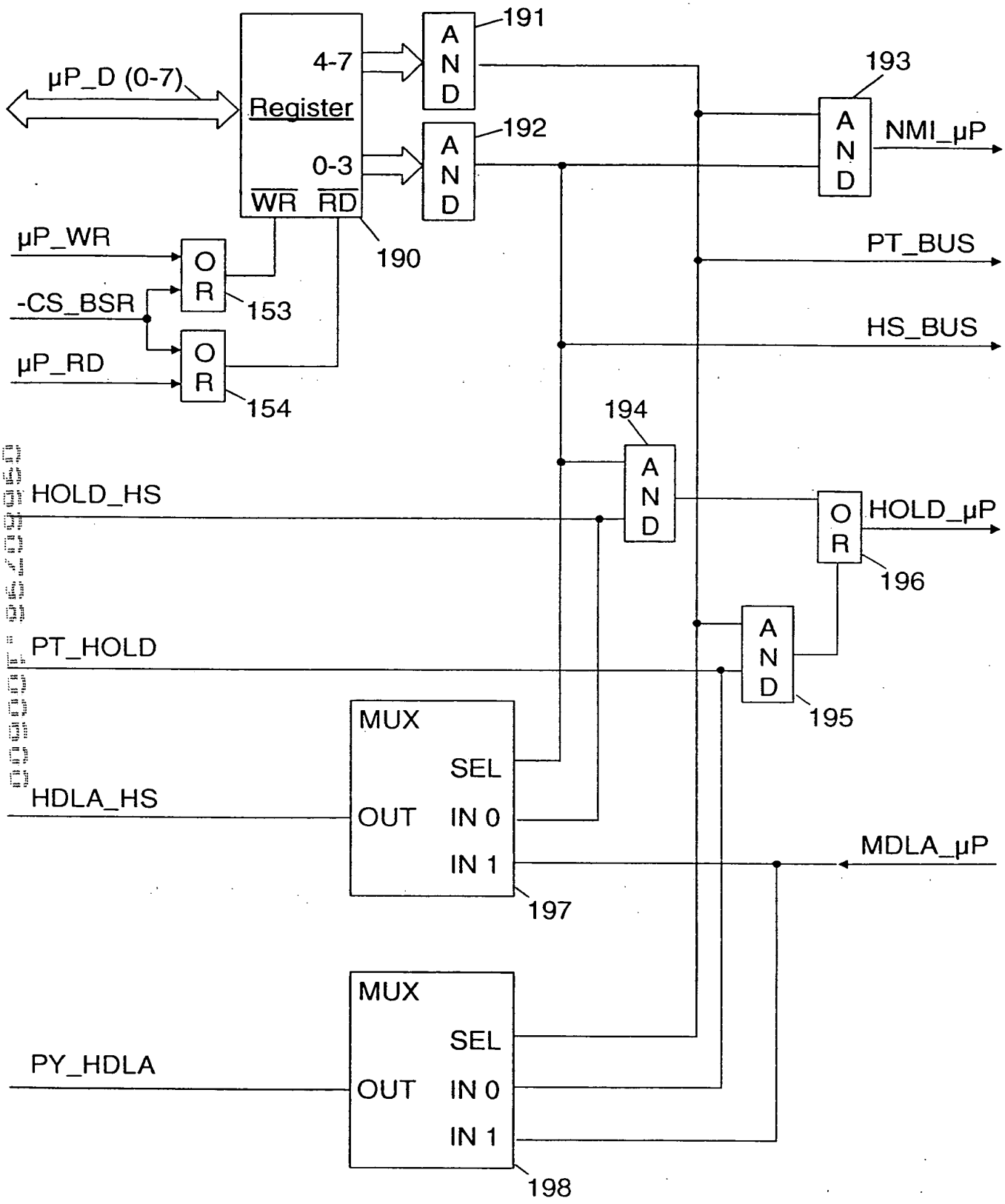
µP_D (0-7)
4-7
Register
0-3
WR
RD
190
191
192
AND
193
AND
NMI_µP
µP_WR
-CS_BSR
µP_RD
OR
153
OR
154
PT_BUS
HS_BUS
194
AND
HOLD_HS
OR
HOLD_µP
196
PT_HOLD
AND
195
MUX
SEL
OUT
IN 0
IN 1
HDLA_HS
MDLA_µP
197
MUX
SEL
PY_HDLA
OUT
IN 0
IN 1
198

FIG. 11

Buffer Description

First address (xxx000H)→ Data byte 01 (managed by first low speed framer)
Data byte 02 (managed by first low speed framer)
Data byte 03 (managed by first low speed framer)
Data byte 04 (managed by first low speed framer)
Data byte 05 (managed by first low speed framer)
Data byte 06 (managed by second low speed framer)
Data byte 07 (managed by second low speed framer)
Data byte 08 (managed by third low speed framer)
Data byte 09 (managed by first low speed framer)
Data byte 10 (managed by first low speed framer)
Data byte 11 (managed by first low speed framer)
Data byte 12 (managed by first low speed framer)
Data byte 13 (managed by first low speed framer)
Data byte 14 (managed by second low speed framer)
Data byte 15 (managed by second low speed framer)
Data byte 16 (managed by third low speed framer)
Data byte 17 (managed by first low speed framer)
Data byte 18 (managed by first low speed framer)

▪
▪
▪

Data byte 2041 (managed by first low speed framer)
Data byte 2042 (managed by first low speed framer)
Data byte 2043 (managed by first low speed framer)
Data byte 2044 (managed by first low speed framer)
Data byte 2045 (managed by first low speed framer)
Data byte 2046 (managed by second low speed framer)
Data byte 2047 (managed by second low speed framer)
Last address (xxx7FFH)→ Data byte 2048 (managed by third low speed framer)

FIG. 12

First Transaction Table

Input address (lowest 11 bits)	Output address (lowest 11 bits)
000	000
001	001
002	002
003	003
004	004
005	008
006	009
007	00A
008	00B
009	00C
00A	010
00B	011
00C	012
00D	013
00E	014
00F	018
010	019
011	01A
. . .	. . .
4FB	7F8
4FC	7F9
4FD	7FA
4FE	7FB
4FF	7FC

FIG. 13

Second Transaction Table

Input address (lowest 11 bits)	Output address (lowest 11 bits)
000	005
001	006
002	00D
003	00E
004	015
005	016
006	01D
007	01E
008	025
009	026
00A	02D
00B	02E
00C	035
00D	036
00E	03D
00F	03E
010	045
011	046
. . .	. . .
1FC	7F5
1FD	7F6
1FE	7FD
1FF	7FE

FIG. 14

Second Transaction Table

Input address (lowest 11 bits)	Output address (lowest 11 bits)
000	007
001	00F
002	017
003	01F
004	027
005	02F
006	037
007	03F
008	047
009	04F
00A	057
00B	05F
00C	067
00D	06F
00E	077
00F	07F
010	087
011	08F
.	.
.	.
.	.
0FC	7F7
0FD	7EF
0FE	7F7
0FF	7FF

FIG. 15

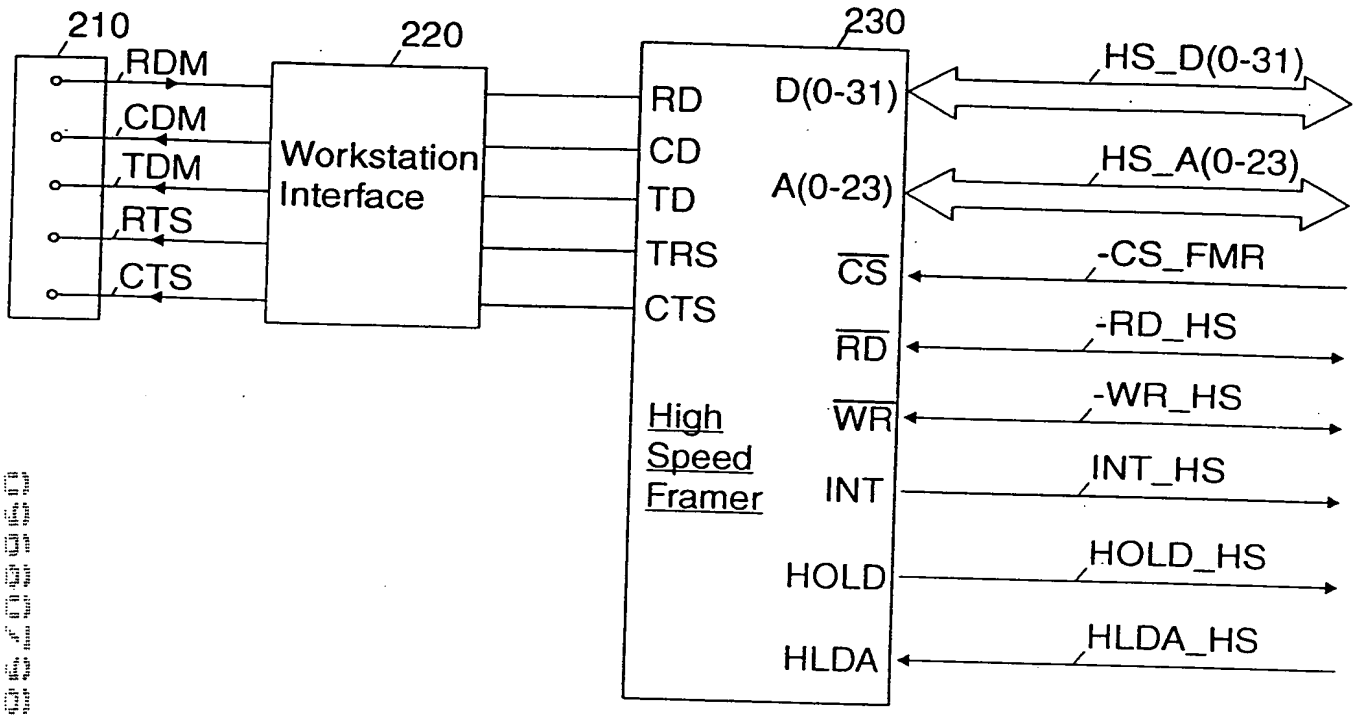
210
RDM
CDM
TDM
RTS
CTS
220
Workstation Interface
230
RD
CD
TD
TRS
CTS
High Speed Framer
D(0-31)
A(0-23)
CS
RD
WR
INT
HOLD
HLDA
HS_D(0-31)
HS_A(0-23)
-CS_FMR
-RD_HS
-WR_HS
INT_HS
HOLD_HS
HLDA_HS

FIG. 16

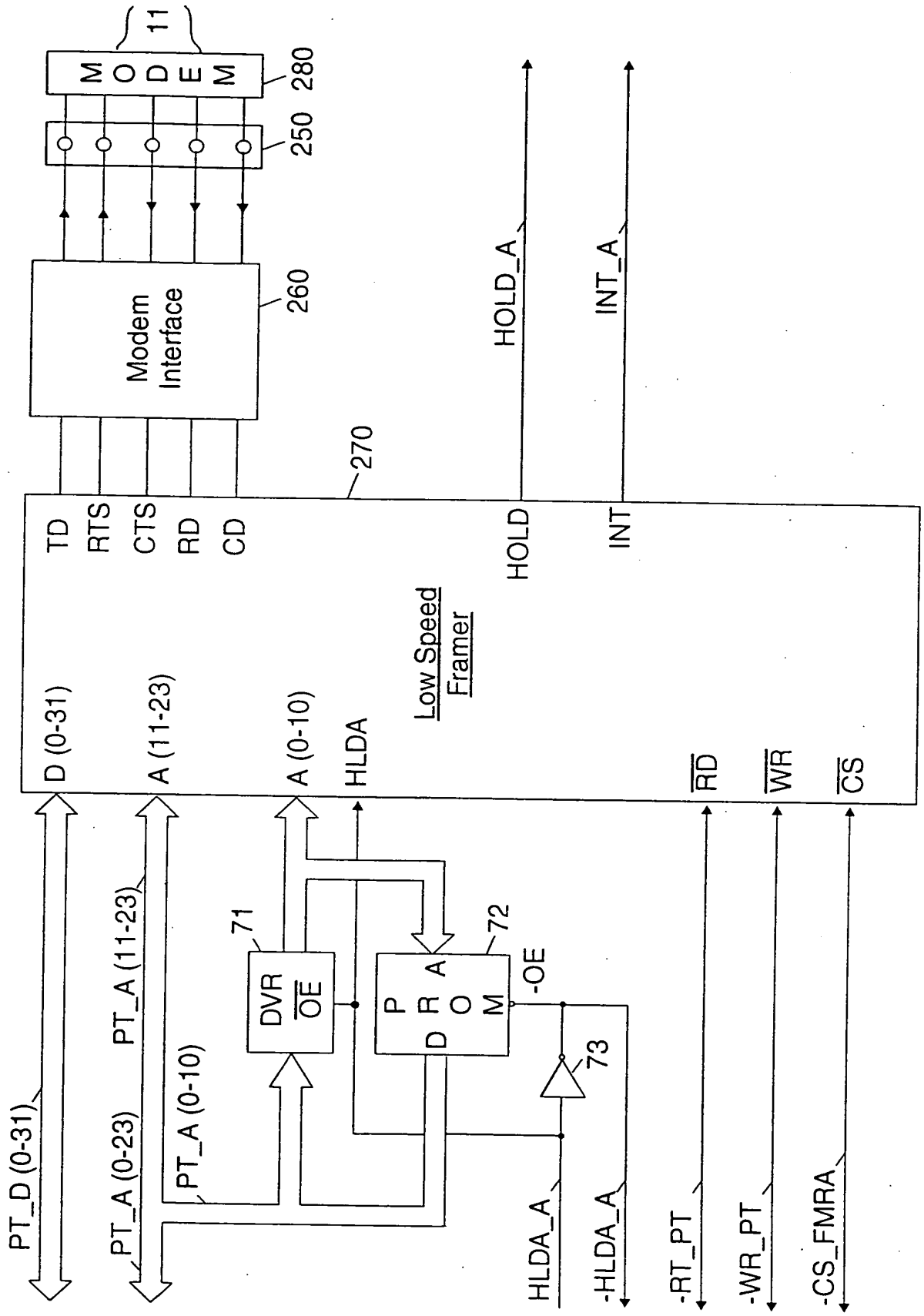
MODEM
11
280
250
Modem Interface
260
HOLD_A
INT_A
270
TD
RTS
CTS
RD
CD
HOLD
INT
Low Speed Framer
D (0-31)
A (11-23)
A (0-10)
HLDA
RD
WR
CS
PT_D (0-31)
PT_A (11-23)
PT_A (0-23)
PT_A (0-10)
71
DVR OE
72
PARO M
-OE
73
HLDA_A
-HLDA_A
-RT_PT
-WR_PT
-CS_FMRA

FIG. 17